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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/465,634	12/17/1999	DAVID K. VAVRO	INTL-0286-US	9115

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TIMOTHY N TROP
TROP PRUNER HU & MILES PC
8554 KATY FREEWAY STE 100
HOUSTON, TX 77024

EXAMINER
DECKTER, STEPHANIE M

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/465,634	VAVRO ET AL.	
	Examiner	Art Unit	
	Stephanie M. Deckter	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 1999 and 18 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 1/18/02 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. However, since those references cited were easily located, the entire IDS has been considered.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 62 as shown in figure 5, 64, 66, and 68 as shown in figure 6, and 110 as shown in figure 13. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites the limitation "wherein said mathematical processor is a multi-cycled mathematical processor." This language is unclear because since the word "cycle" is a

measurement of time, it is unclear how a processor can be multi-timed. This phraseology may mean the processor requires multiple cycles to complete an operation or that it is operated at various cycle speeds. For purposes of examination, the former meaning will be assumed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-4, 6, 8, 9, 15, 16, 17, 23, and 24 are rejected under 35 U.S.C. 102(a) as being anticipated by Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura). Referring to claim 1, Kitamura has taught a digital signal processor comprising:

a. a mathematical processor (Kitamura column 9, line 58 to column 10, line 1 and figure 6, element 5);

b. an input processor that processes input signals to the digital signal processor (Kitamura column 10, line 28 to column 11, line 8 and figure 6, element 3);

c. an output processor that processes output signals from the digital signal processor (Kitamura column 12, lines 15-52 and figure 6, element 6);

d. a master processor that controls said mathematical processor, said input processor and said output processor (Kitamura column 10, lines 1-2 and figure 6, element 7); and

e. a storage selectively accessible by each of said processors (Kitamura column 10, lines 21-27 and figure 6, element 10).

7. Referring to claim 2, Kitamura has taught the digital signal processor further including a random access memory processor that stores intermediate calculation results (Kitamura column 12, lines 10-14).

8. Referring to claim 3, Kitamura has taught the digital signal processor including a bus coupling each of said processors to said storage (Kitamura figure 6, element 9).

9. Referring to claim 4, Kitamura has taught the digital signal processor wherein said input and output processors also implement mathematical operations (Kitamura column 10, line 28 to column 11, line 8, column 12, lines 15-52 and figure 6, elements 3 and 6).

10. Referring to claim 6, Kitamura has taught the digital signal processor wherein said processors communicate with one another through said storage (Kitamura column 10, lines 15-17 and 28-32, column 11, lines 47-55, and column 12, lines 15-20).

11. Referring to claim 8, Kitamura has taught the digital signal processor wherein said master processor provides the timing for the other processors (Kitamura column 10, lines 5-14 where the master processor determines the timing for when the processors execute instructions because it controls when the instructions are sent).

12. Referring to claim 9, Kitamura has taught the digital signal processor wherein said master processor waits for the input processor to complete a given operation (Kitamura column 6, lines 3-20 and column 11, lines 47-49 where the signal must be processed in the input processor before being spliced by the data processing unit as per the control of the master processor, therefore, the master processor must wait for the input processor to complete its operation).

13. Referring to claim 15, Kitamura has taught the digital signal processor wherein said mathematical processor is a multi-cycled mathematical processor (Kitamura column 11, lines 46-55 where an operation takes multiple cycles to complete).

14. Claim 16 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

15. Claim 17 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

16. Claims 23 and 24 do not recite limitations above the claimed invention set forth in claim 15 and are therefore rejected for the same reasons set forth in the rejection of claim 15 above.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 5, 7, 14, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura). Referring to claim 5, Kitamura has not explicitly taught each of said processors having their own instruction sets. However, Kitamura has taught a mathematical processor, an input processor, an output processor, and a master processor each with divergent functionality. Since the definition of an instruction set is that combination of commands which allows a processor to appropriately perform its defined functions, it would be readily acknowledged by an artisan that the plural processors as taught by Kitamura must each have their own instruction set. That is, the

instructions required to perform the input processing, mathematical functions, control, and output processing must be different from one another. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recreate the plural processors of Kitamura where each has its own instruction set. Official notice has been taken.

19. Referring to claim 7, Kitamura has not explicitly taught each processor using very long instruction words. Employing this type of instruction format is well known in the art and would have allowed for the processors of Kitamura to be issued several instructions at once and ensured, by the nature of VLIW instructions, that the compiler would have only combined instructions that are not dependent upon one another. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the very long instruction word format for instructions issued to the plural processors of Kitamura in order to increase speed and efficiency of those processors. Official notice has been taken.

20. Referring to claim 14, Kitamura has not explicitly taught a mathematical pipeline which is pipelined. However, Kitamura has taught a mathematical processor that requires multiple cycles to complete a given operation, i.e. at least one cycle for memory access and one cycle for execution (Kitamura column 11, lines 51-55). The concept of pipelining is well known in the art and would have been beneficially employed in the mathematical processor of Kitamura in order to increase efficiency by overlapping the steps of memory access and execution for each processed instruction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the well known concept of pipelining to the mathematical processor in order to increase efficiency and speedup. Official notice has been taken.

21. Claim 22 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

22. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura) in view of Whittaker et al., U.S. Patent Number 5,968,167 (hereinafter Whittaker). Kitamura has not explicitly taught the digital signal processor wherein each of said processors includes its own random access memory. Whittaker has taught each of a plurality of processors including its own random access memory (Whittaker column 6, lines 56-65). The RAMs of Whittaker provide storage for those instructions to be executed by each processor. As discussed above in the rejection of claim 5, each processor of Kitamura has its own instruction set and those instructions are issued to each processor by the master processor. Therefore, it would have been beneficial to employ separate RAMs for each processor such that the master processor would have required less logic to inform each processor to access its RAM and fetch its own next instruction, rather than the master accessing the main storage, determining which processor the instruction belonged to, and then physically issuing that instruction to the slave processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ individual RAMs for each of the plural processors of Kitamura, as taught by Whittaker in order to allow for a simpler master processor.

23. Claims 11-13, 18-21, and 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, EP 0942603A2 as labeled document I in Applicant's IDS (hereinafter Kitamura) in view of Nakagawa et al., U.S. Patent Number 5,241,679 (hereinafter Nakagawa). Referring to claim 11, Kitamura has not taught the digital signal processor wherein

said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register. Nakagawa has taught a storage including a plurality of registers (Nakagawa figure 1), where the registers automatically transfer existing data from a first register to a second register when new data is written into the first register (Nakagawa column 4, line 53 to column 5, line 16 and figure 2). Replacing the storage of Kitamura with the multi-register storage of Nakagawa would have allowed for the contents of all the registers to be saved, in case of an interrupt or context switch, simultaneously to the dedicated stack memories in order to perform both saving and restoration at a high speed (Nakagawa column 2, lines 17-23 and 42-49). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the multi-register storage system of Nakagawa instead of the generic storage means in the system of Kitamura in order to increase the speed at which context preserving and restoration occurs.

24. Referring to claim 12, Nakagawa has taught the digital signal processor wherein said input processor causes the automatic transfer of data (Nakagawa column 4, line 53 to column 5, line 16 where the processor causing the data to be stored is necessarily an input processor).

25. Referring to claim 13, Nakagawa has taught the digital signal processor wherein the mathematical processor causes said data to be transferred from one register to another (Nakagawa column 4, line 53 to column 5, line 16).

26. Claim 18 does not recite limitations above the claimed invention set forth in claim 11 and is therefore rejected for the same reasons set forth in the rejection of claim 11 above.

27. Claim 19 does not recite limitations above the claimed invention set forth in claim 12 and is therefore rejected for the same reasons set forth in the rejection of claim 12 above.

28. Claim 20 does not recite limitations above the claimed invention set forth in claim 13 and is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

29. Referring to claim 21, Nakagawa has taught storing a bit which indicates which processor may controls aid automatic transfer of data from one register to another (Nakagawa column 2, lines 29-33).

30. Referring to claim 25, Kitamura has taught a method comprising:

a. digital signal processing input data (Kitamura column 10, lines 28-30).

Kitamura has not taught in response to a write request to a first register, automatically transferring data from a first register to a second register. Nakagawa has taught such (Nakagawa column 4, line 53 to column 5, line 16 and figure 2). Replacing the storage of Kitamura with the multi-register storage of Nakagawa would have allowed for the contents of all the registers to be saved, in case of an interrupt or context switch, simultaneously to the dedicated stack memories in order to perform both saving and restoration at a high speed (Nakagawa column 2, lines 17-23 and 42-49). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the multi-register storage system of Nakagawa instead of the generic storage means in the system of Kitamura to ensure that data would be automatically transferred from first to second registers in response to a write request on the first register, in order to increase the speed at which context preserving and restoration occurs.

31. Referring to claim 26, Nakagawa has taught automatically transferring data from said second register to a third register in response to the transfer of data from said first register to said second register (Nakagawa column 4, line 53 to column 5, line 16 and figure 2).

32. Referring to claim 27, Kitamura has taught the method including using a plurality of parallel processors to process said data (Kitamura figure 6, elements 3, 5, 6, and 7). Kitamura has not taught storing information to control which processors can cause the automatic transfer of data. However, Nakagawa has taught a bit which indicates control of the automatic transfer of data (Nakagawa column 2, lines 29-33). When more than one processor may control data storage, the system requires a method to control which processor can do so and when. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to store information regarding the plural processors of Kitamura within the instruction code bit of Nakagawa to determine which processor may control the automatic transfer of data.

33. Claim 28 does not recite limitations above the claimed invention set forth in claim 25 and is therefore rejected for the same reasons set forth in the rejection of claim 25 above.

34. Claim 29 does not recite limitations above the claimed invention set forth in claim 26 and is therefore rejected for the same reasons set forth in the rejection of claim 26 above.

35. Claim 30 does not recite limitations above the claimed invention set forth in claim 27 and is therefore rejected for the same reasons set forth in the rejection of claim 27 above.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Hansen et al., U.S. Patent Number 5,742,840, have taught a digital signal processor comprising mathematical, input, output, and master processors, as well as a shared storage.

Yamamoto et al., U.S. Patent Number 6,397,321, have taught a digital signal processor comprising mathematical, input, output, and master processors, as well as a shared storage and a storage for holding intermediate calculation results.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephanie M. Deckter whose telephone number is 703-308-6132. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Stephanie M. Deckter
Examiner
Art Unit 2183 SMD

July 1, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100